REMARKS

The abstract of the disclosure is objected to for reasons stated in the Office Action at page 2. The abstract is amended to reduce the total word count to fewer than 150 words. Entry of the amendments to the abstract and removal of the objection are respectfully requested.

The drawings are objected to for reasons stated in the Office Action at page 2. Figures 1-4E of the drawings are amended to include the legend "PRIOR ART." Reconsideration of the objections to the drawings is respectfully requested.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Morita (United States Publication Number 2002/0196243 A1). Claims 1-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita in view of Hirai, *et al.* (United States Patent Number 5,953,002).

Applicant submits that the rejection of claim 12 under 35 U.S.C. 102(b) based on Morita is improper, because Morita was described in a printed publication on December 26, 2002, which is less than one year prior to the United States filing date of the present application (November 13, 2003). Notwithstanding the foregoing, the amendments to the claims and the following remarks assume that the Morita reference is qualified as a prior art reference under 35 U.S.C. 102(e). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections of claims 1-13 is respectfully requested.

The present invention according to amended independent claim 1 is directed to a super twisted nematic (STN) liquid crystal display (LCD) driver comprising a sub frame counter, an N clock counter, a frame counter, and a liquid crystal polarity inversion signal generator. The sub frame counter counts a number of sub frames in a frame in response to a clock signal and generates a sub frame flag signal every time each sub frame is counted in the frame. The N clock counter receives an N-line signal and generates an N-line flag signal every time the number of N-lines counted is N in response to the clock signal. The frame counter receives a frame rate control (FRC) selection signal, counts the number of the sub frame flag signal received from the sub frame counter, and generates a frame flag signal every time the number of the sub frame flag signal counted is n. The liquid crystal polarity inversion signal generator receives one of the sub

frame flag signal, the N-line flag signal, and the frame flag signal in response to a selection signal, and generates a liquid crystal polarity inversion signal that inverts a polarity of an STN LCD.

The present invention according to amended independent claim 5 is directed to a driving method of a super twisted nematic (STN) liquid crystal display (LCD) driver. A number of sub frames in a frame is counted in response to a clock signal and generating a sub frame flag signal every time each sub frame is counted in the frame. An N-line signal is received and an N-line flag signal is generated in response to input of the clock signal every time the number of N-line counted is N in response to the clock signal. A frame rate control (FRC) selection signal is received, the number of sub frame flag signals received from the sub frame counter is counted, and a frame flag signal is generated every time the number of sub frame flag signals counted is n. One of the sub frame flag signal, the N-line flag signal, and the frame flag signal is selected in response to a selection signal, and generating a liquid crystal polarity inversion signal that inverts a polarity of the STN LCD.

The present invention according to amended independent claim 9 is directed to a driving method of a super twisted nematic (STN) liquid crystal display (LCD) driver. A frame rate control (FRC) selection signal is determined is in accordance with an nFRC method. A number of sub frames in a frame is counted. A liquid crystal polarity inversion signal in the frame is generated that inverts a polarity of an STN LCD if the number of sub frames in the frame is n.

The present invention according to amended independent claim 12 is directed to a driving method of a super twisted nematic (STN) liquid crystal display (LCD) driver using an nFRC method, wherein a polarity of an STN LCD is inverted in each frame.

It is submitted that Morita and Hirai, *et al.*, alone or in combination, fail to teach or suggest a super twisted nematic (STN) liquid crystal display (LCD) driver comprising a sub frame counter, which counts a number of sub frames in a frame in response to a clock signal and generates a sub frame flag signal every time each sub frame is counted in the frame, as claimed in amended independent claim 1.

Morita fails to teach or suggest a super twisted nematic (STN) liquid crystal display (LCD) driver, as claimed. Instead, Morita discloses a display control circuit for a TFT liquid crystal display (see Morita Abstract and page 3, paragraphs [0063]- [0064]). Moreover, Morita

distinguishes the TFT LCD of Morita as being different than an STN LCD, for reasons stated at page 3, paragraph [0063] and pages 14-15, paragraph [290] of the Morita reference.

However, the Office Action at page 4, lines 4-6 refers to Morita as comprising a sub frame counter. However, close inspection of Morita reveals that Morita discloses frame counters (see Morita, page 16, paragraphs [0315], [0327]), not a sub frame counter. Specifically, there is no teaching or suggestion that the frame counter disclosed in Morita is the Applicant's claimed sub frame counter, since the frame counter of Morita does not count a number of sub frames in a frame in response to a clock signal, as claimed. In addition, there is no teaching or suggestion in Morita of the frame counter of Morita generating a sub frame flag signal every time each sub frame is counted in the frame, as claimed.

Hirai, *et al.* discloses a driving method for a direct addressing type LCD device for displaying gradation by changing the amplitude of voltages applied to pixels, wherein the voltages are made constant in a display frame period (see Hirai, Abstract and column 4, lines 36-46). To achieve this, Hirai, *et al.* discloses in part a circuit for driving an LCD device that includes sub frame counters (see Hirai, Figure 4). However, close inspection of Hirai, *et al.* reveals that there is likewise no teaching or suggestion in Hirai, *et al.* of a sub frame counter, which counts a number of sub frames in a frame in response to a clock signal and generates a sub frame flag signal every time each sub frame is counted in a frame, as claimed in amended independent claim 1. Instead, Hirai, *et al.* teaches that frame-distributed signals are output in synchronism with the sub frame counters to display data for each sub frame in a 3-bit parallel form (see Hirai, column 14, lines 37-39). However, there is no teaching or suggestion that the frame-distributed signals output in synchronism sub frame counters in Hirai, *et al.* are generated as a sub frame flag signal every time each sub frame is counted in a frame, as claimed in amended independent claim 1.

Moreover, even if the sub frame counter in Hirai, *et al.* was an analog of the Applicant's claimed sub frame counter, the Applicant respectfully believes that the combination of Hirai, *et al.* and Morita is improper under 35 U.S.C. § 103(a) because there is no explicit teaching or suggestion in Hirai, *et al.* and Morita that would motivate one skilled in the art to apply the sub frame counter of Hirai, *et al.* to the abovementioned display control circuit of Morita. Morita does not teach or suggest a super twisted nematic (STN) liquid crystal display (LCD) driver, but,

as described above, Morita instead teaches a display control circuit for a TFT liquid crystal display. Morever, there is no teaching or suggestion in Morita of sub frames being formed by the display control circuit of Morita, and therefore, there is no teaching in Morita of a sub frame counter. Hirai, *et al.*, on the other hand, discloses a sub frame counter that is used in a driving method for a passive addressing type liquid crystal display device (see Hirai, column 1, lines 6-7). However, a direct addressing type liquid crystal display device, such as the device of Hirai, *et al.*, does not use active elements such as TFTs, as disclosed in Morita (see Hirai, column 1, lines 16-20). Therefore, one of skill in the art would in no way be motivated to combine the sub frame counter of Hirai, *et al.* with the TFT liquid crystal display of Morita.

In addition, it is submitted that Morita and Hirai, *et al.*, alone or in combination, fail to teach or suggest a frame counter, which receives a frame rate control (FRC) selection signal, counts a number of a sub frame flag signal, and generates a frame flag signal every time the number of the sub frame flag signal counted is n, as claimed in amended independent claim 1. Specifically, since neither Morita nor Hirai, *et al.* teaches or suggests a sub frame counter that generates a sub frame flag signal every time each sub frame is counted in a frame, as claimed, it follows that neither Morita nor Hirai, *et al.* teaches or suggests a frame counter that counts a number of a sub frame flag signal, as claimed.

In addition, it is submitted that Morita and Hirai, *et al.*, alone or in combination, fail to teach or suggest an N clock counter, which receives an N-line signal and generates an N-line flag signal every time a number of N-lines counted is N in response to a clock signal, as claimed.

With regard to Morita, Morita discloses a polarity inverting signal FR that is supplied for every frame, and a timing signal VCOM that inverts the polarity of a common electrode and a signal to be inverted in synchronism with the polarity inverting signal FR (see Morita, Figure 21 and page 16, paragraph [0326]). In addition, a signal FULLSCAN is generated for performing a full scan (see Morita, page 16, paragraph [0326]). However, there is no teaching or suggestion in Morita that the abovementioned signals are an N-line flag signal generated by an N clock counter, and generated every time a number of N-lines counted is N in response to a clock signal, as claimed.

With regard to Hirai, *et al.*, there is likewise no teaching or suggestion of an N clock counter, which receives an N-line signal and generates an N-line flag signal every time a number

of N-lines counted is N in response to a clock signal, as claimed.

In addition, it is submitted that Morita and Hirai, *et al.*, alone or in combination, fail to teach or suggest a liquid crystal polarity inversion signal generator, which receives one of a sub frame flag signal, a N-line flag signal, and a frame flag signal in response to a selection signal, and generates a liquid crystal polarity inversion signal that inverts a polarity of an STN LCD, as claimed in amended independent claim 1. Neither Morita and Hirai, *et al.* teaches or suggests a sub frame counter that generates a sub frame signal, as claimed. In addition, neither Morita and Hirai, *et al.* teaches or suggests an N clock counter that generates an N-line flag signal, as claimed. In addition, neither Morita and Hirai, *et al.* teaches or suggests a frame counter that generates a flag signal, as claimed. Since neither Morita and Hirai, *et al.* teaches a sub frame signal, N-line flag signal, or a flag signal, as claimed, it follows that neither Morita and Hirai, *et al.* teaches or suggests a liquid crystal polarity inversion signal generator, which receives one of a sub frame flag signal, a N-line flag signal, and a frame flag signal in response to a selection signal, as claimed.

With regard to the rejection of amended independent claim 5, it is submitted that the combination of Morita and Hirai, *et al.* fails to teach or suggest counting a number of sub frames in a frame in response to a clock signal and generating a sub frame flag signal every time each sub frame is counted in the frame, as claimed in amended independent claim 5, for reasons at least similar to those described above.

In addition, it is submitted that the combination of Morita and Hirai, *et al.* fails to teach or suggest receiving a frame rate control (FRC) selection signal, counting a number of sub frame flag signals received from a sub frame counter, and generating a frame flag signal every time the number of sub frame flag signals counted is n, as claimed in amended independent claim 5, for reasons at least similar to those described above.

In addition, it is submitted that the combination of Morita and Hirai, *et al.* fails to teach or suggest receiving an N-line signal and generating an N-line flag signal in response to input of an clock signal every time a number of N-lines counted is N in response to a clock signal, as claimed in amended independent claim 5, for reasons at least similar to those described above.

In addition, it is submitted that the combination of Morita and Hirai, *et al.* fails to teach or suggest selecting one of a sub frame flag signal, a N-line flag signal, and a frame flag signal in

response to a selection signal, and generating a liquid crystal polarity inversion signal that inverts a polarity of the STN LCD, as claimed in amended independent claim 5, for reasons at least similar to those described above.

With regard to the rejection of amended independent claim 9, it is submitted that the combination of Morita and Hirai, *et al.* fails to teach or suggest generating a liquid crystal polarity inversion signal in a frame that inverts a polarity of an STN LCD if a number of sub frames in the frame is n, as claimed in amended independent claim 1, for reasons at least similar to those described above. In addition, with regard to Hirai, *et al.*, Hirai, *et al.* specifically discloses that a polarity of data signals is inverted after two frames (4 sub frames) have been completed (see Hirai, column 33, lines 1-2). There is no teaching or suggestion in Hirai, *et al.* of the polarity of data signals being inverted if a number of sub frames in a frame is n, as claimed in amended independent claim 9.

It is therefore submitted that Morita and Hirai, *et al.* fail to teach or suggest the invention set forth in the amended claims. Since Morita and Hirai, *et al.* fails to teach or suggest these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since the combination of Morita and Hirai, *et al.* fails to teach or suggest the invention set forth in the amended claims, claims 1-11 and 13 are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 1-11 and 13 under 35 U.S.C. 103(a) based on the combination of Morita and Hirai, *et al.* are respectfully requested.

With regard to the rejection of amended independent claim 12 under 35 U.S.C. 102(b) based on Morita, it is submitted that Morita fails to teach or suggest a driving method of a super twisted nematic (STN) liquid crystal display (LCD) driver using an nFRC method, wherein a polarity of an STN LCD is inverted in each frame, as claimed in amended independent claim 12, for reasons at least similar to those described above. Reconsideration of the rejection of claim 12 under 35 U.S.C. 102(b) based on Morita is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all

claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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FIG. 1 (PRIOR ART)

LIQUID CRYSTAL POLARITY INVERSION SIGNAL M	H		L	
	COM VOLTAGE (VCOM)	SEGMENT VOLTAGE (VSEG)	COM VOLTAGE (VCOM)	SEGMENT VOLTAGE (VSEG)
SELECTION	VSS	V0	V0	VSS
NON-SELECTION	V1	V2	V4	V3

FIG. 2 (PRIOR ART)

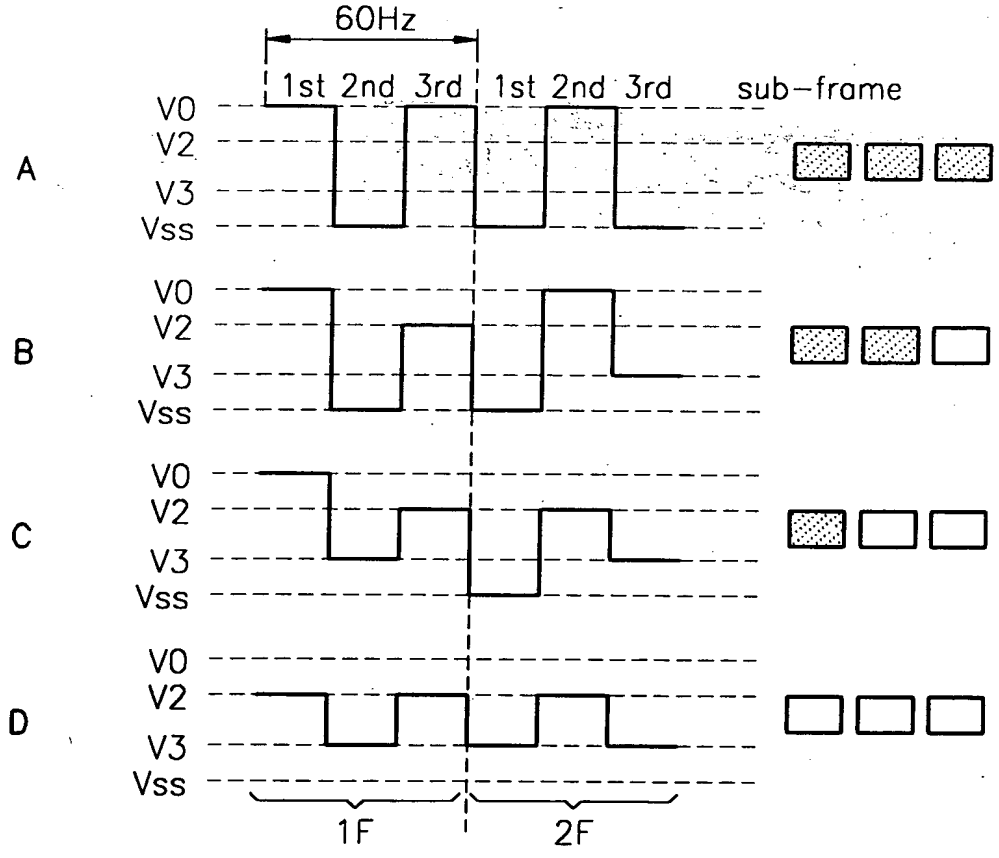

FIG. 3 (PRIOR ART)

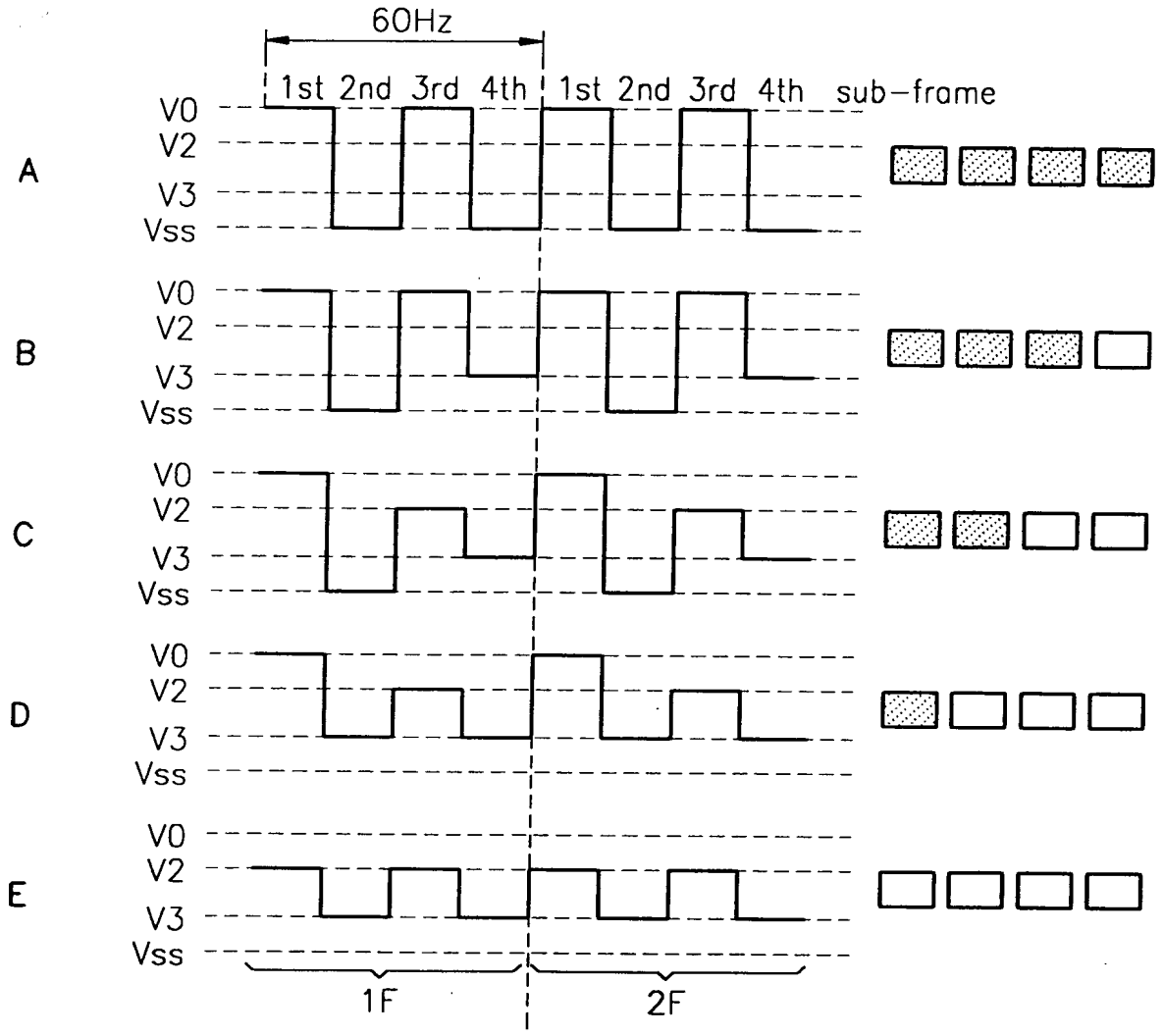

FIG. 4 (PRIOR ART)